

Physical Design Engineer

Designation:
Physical Design Engineer

Experience Level:
3+ years of hands-on physical design flows.

Responsibilities:

Block level and or Chip level synthesis, place and route, end to end execution from floor planning to PV closure.

Own the blocks for physical design activities of synthesis, Floor planning, place and route, CTS, STA and Timing closure.

Should be able to complete physical design activities under minimal guidance.

Requirements:

Bachelors/Masters in ECE from a reputed University.

Experience in EDA synthesis, APR, STA tools and methodologies

Experience in one or more of the following tools

ICC, ICC2, Innovus, Olympus.

Working knowledge of one or more of the following tools

Primetime, Calibre, and Red hawk.

Hands on experience of working with multi modes and multi corners STA.

Working Knowledge of multiple power planes and multiple VT libraries.

Basic domain knowledge of EM, IR, RV analysis, Noise and Formal Equivalence Verification.

Good at scripting languages PERL, TCL, shell.

Worked on at least 2 tape ins of moderate to high speed designs. With multiple power planes.

Debug, fix, and validate pre- and post-silicon IP/sub-system logic issues and bugs.

Experience in one or more of the following circuit design fields is an advantage:
clock tree optimization, Timing analysis, and Power optimization.

Experience in making ECOs both Metal and logic level ecos.

Experience DRC and LVS cleanup of designs during sign off.

Exposure to lower node technologies 16nm or below preferred.

Good Analytical and Debug skills required.

Additional knowledge:

Experienced on working with primarily Verilog (but also VHDL and System Verilog) RTL design.

FPGA prototyping experience a plus

Basic knowledge of VLSI circuit design fundamentals

Basic Knowledge of CMOS Logic, high-speed, low-power digital circuits, concepts of timing and physical design convergence.

Excellent written and verbal communication in English.

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